FORM PTO-875
Rev. 3-83

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION FEE DETERMINATION RECORD

SERIAL NO.	FILING DATE
218,312	2-12-88
APPLICANT (FIRST NAMED)	
Holmberg	

CLAIMS AS FILED - PART I

FOR	NO. FILED		NO. EXTRA
BASIC FEE			
TOTAL CLAIMS	36	- 20 =	16
INDEP. CLAIMS	4	- 3 =	1
MULTIPLE DEPENDENT CLAIM PRESENT			

* If the difference in col. 1 is less than zero, enter "0" in col. 2

SMALL ENTITY			OTHER THAN A SMALL ENTITY	
RATE	FEE		RATE	FEE
	$170	OR		$340
x6	$	OR	x12	$192
x17	$	OR	x34	$34
x55	$	OR	x110	$
TOTAL	$	OR	TOTAL	$526

CLAIMS AS AMENDED - PART II

	(1)		(2)	(3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
AMENDMENT A				
TOTAL	*	MINUS	**	*
INDEP.	*	MINUS	***	*
FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY			OTHER THAN A SMALL ENTITY	
RATE	ADDIT. FEE		RATE	ADDIT. FEE
x9	$	OR	x18	$
x19	$	OR	x38	$
x50	$	OR	x100	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

	(1)		(2)	(3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
AMENDMENT B				
TOTAL	*	MINUS	**	*
INDEP.	*	MINUS	***	*
FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY			OTHER THAN A SMALL ENTITY	
RATE	ADDIT. FEE		RATE	ADDIT. FEE
x9	$	OR	x18	$
x19	$	OR	x38	$
x50	$	OR	x100	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

	(1)		(2)	(3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA
AMENDMENT C				
TOTAL	*	MINUS	**	*
INDEP.	*	MINUS	***	*
FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY			OTHER THAN A SMALL ENTITY	
RATE	ADDIT. FEE		RATE	ADDIT. FEE
x9	$	OR	x18	$
x19	$	OR	x38	$
x50	$	OR	x100	$
TOTAL ADDIT. FEE	$	OR	TOTAL	$

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.

** If the Highest No. Previously Paid For IN THIS SPACE is less than 20, enter "20".

*** If the Highest No. Previously Paid For IN THIS SPACE is less than 3, enter "3".

The "Highest No. Previously Paid For" (Total or Indep.) is the highest number found in the appropriate box in Col. 1.

manufacture thereof; Karl J. Youtsey, et al., 427/91; 252*500, 502; 357*8; 427*122, 215, 220, 221, 228, 249, 255, 384, 385.5

23. 3,922,364, Nov. 25, 1975, Electrically conductive [illegible]bers; Thomas D. Tadewald, 427*126.1; 65*3.44, 60.3; 427*185, 204; 428*632; 427/235

24. 3,916,509, Nov. 4, 1975, Method of manufacturing a semi-conductor target for a camera tube having a mosaic of p-n junctions covered by a perforated conductive layer; Arthur Marie Eugene Hoeberechts, et al., 29/583; 357*56; 427/95, 96, 141, 153, 216

25. 3,884,688, May 20, 1975, Photosensitive element employing a vitreous bismuth-selenium film; John C. Schottmiller, et al., 428*457; 313*385; 430*84; 427/232, 216; 505*849

26. 3,874,917, Apr. 1, 1975, Method of forming vitreous semiconductors by vapor depositing bismuth and selenium; Charles Wood, et al., 427/53; 427*76, 160; 428*426, 446, 523; 427/232

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US-PAT-NO: [redacted] L2: 4 of 26
US-CL-CURRENT: 427/42, 255, 238

ABSTRACT:
A . . . charge density and a higher dielectric breakdown strength, is applicable to wide variety of MOSFET applications, and is inherently less electrostatic discharge (ESD) sensitive than conventional gate structures due to the distributed electric field.

SUMMARY:

3. 4,581,538, Jan. 31, 1987, Electrostatic discharge protection using thin nickel fuse; Arturo Simmons, et al., 4573170; 148*DIG.55; 357*30; 43795, 22, 922

4. 4,791,071, Dec. 13, 1988, Dual dielectric gate system comprising silicon dioxide and amorphous silicon; Saw T. Ang, 437242, 235, 238

5. 4,762,802, Aug. 9, 1988, Method for preventing latchup in CMOS devices; Louis C. Parrillo, 437224; 148*DIG.82; 357*42, 91; 437228, 29, 34

6. 4,760,031, Jul. 26, 1988, Producing CCD imaging sensor with flashed backside metal film; James R. Janesick, 43733; 357*24; 437253, 181, 195, 203, 225

7. 4,624,862, Nov. 25, 1986, Boron doped semiconductor materials and method for producing same; Chi C. Yang, et al., 427*74; 136*258; 43722, 81, 301

8. 4,622,574, Nov. 11, 1986, Semiconductor chip with recessed bond pads; Enrique Garcia, 357*55, 56; 428*209; 437204, 225

9. 4,566,242, May 6, 1986, Operations on a semiconductor integrated circuit having two kinds of buffers, Marc L. Harrison, 43738, 170

10. 4,574,466, Mar. 11, 1986, High quality gate oxides for VLSI devices; George F. Hagner, et al., 437225; 148*DIG.81, DIG.118; 156*657; 427*255.4; 437228

11. 4,534,099, Aug. 13, 1985, Method of making multilayer photoelectrodes and photovoltaic cells; Arthur T. Howe, 43732; 148*DIG.20, DIG.118; 357*67, 71; 427*74; 437180, 181, 190, 192, 200

12. 4,520,010, May 28, 1985, Process for modifying the electrical properties of selenium, and selenium alloys; Santokh S. Badesha, et al., 437232; 75*121; 423*508, 510; 427*74, 207.1

13. 4,471,369, Sep. 11, 1984, Robotic pressure imagers; Thomas R. Anthony, et al., 357*26; 73*862.04; 357*51, 55; 437201

14. 4,463,216, Jul. 31, 1984, Solar cell; Hirotaka Nakano, et al., 136*256; 357*30, 52, 54; 43702, 236

15. 4,455,739, Jun. 26, 1984, Process protection for individual device gates on large area MIS devices; Jaroslav Hynecek, 437170, 8, 205, 226

16. 4,370,175, Jan. 25, 1983, Method of annealing implanted semiconductors by lasers; Jeffrey I. Levatter, 43732; 148*DIG.90, DIG.92, DIG.93;

219*121.6; 357*30, 91; 427*53.1; 437219, 22, 936, 949

17. 4,359,512, Nov. 16, 1982, Layered photoconductive member having barrier of silicon and halogen; Tadaji Fukuda, et al., 430*57, 58, 65, 130, 132, 900; 43704

18. 4,234,361, Nov. 18, 1980, Process for producing an electrostatically deformable thin silicon membranes utilizing a two-stage diffusion step to form an etchant resistant layer; Henry Guckel, et al., 437165; 29*621.1; 156*628, 648, 657, 662, 338*2, 4; 357*4, 26, 55, 60; 437228

19. 4,225,222, Sep. 30, 1980, Printing drum for an electrostatic imaging process with a doped amorphous silicon layer; Karl Kempter, 355*3DR; 427*39; 430*57, 95, 133, 135, 136; 437101

20. 4,139,935, Feb. 20, 1979, Over voltage protective device and circuits

for insulated gate transistors; Claude L. Bertin, et al., 437912; 357*13, 23.13, 41, 91; 437944, 52, 165

21. 4,102,714, Jul. 25, 1978, Process for fabricating a low breakdown voltage device for polysilicon gate technology; David E. DeBar, et al., 437959; 148*DIG.168; 156*6[redacted] 653, 657, 662; 357*13, 2[redacted] 23.9, 41, 55, 59, 60; 437909, 228, 904

22. 3,940,509, Feb. 24, 1976, Semi-conducting materials and a method for the